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COER University

END SEMESTER EXAMINATION, EVEN SEM 2022-23 (BACK PAPER)

Time : 3 hours
Program Name : BCA
Course Name : Basics of Digital Electronics

Total Marks : 100
Semester : II
Course Code : SOC156

Note: All questions are compulsory. No student is allowed to leave the examination hall before the completion of the time.

Q. No 1	Attempt Any Four Parts. Each Question Carries 5 Marks.	CO	BL
(a)	What is parity? Explain even and odd parity methods with their respective truth tables for 4-bit data.	CO 1	2,3
(b)	Convert the following numbers as indicated; a) $(111110101)_2 = (?)_{10}$ b) $(476.23)_{10} = (?)_8$ c) $(B9C.24D)_{16} = (?)_2$	CO 1	3
(c)	What is multiplexer tree? Design 32:1 MUX by using 8:1 MUX and 2:1 MUX.	CO 1	2,4
(d)	Convert the 187 decimal number to 8-bit binary and 111111110010 to hexadecimal.	CO 1	3
(e)	Find the Excess 3 code for decimal number 81.61	CO 1	3

Q. No 2	Attempt Any Four Parts. Each Question Carries 5 Marks.	CO	BL
(a)	Differentiate 1's and 2's complement methods of subtraction. Subtract following by using 1's and 2's complement methods of subtraction; i) $(1101)_2 - (1001)_2$ ii) $(33)_{10} - (27)_{10}$	CO 2	2,3
(b)	Subtract the following numbers by using respective complement methods of subtraction: i) $(1100)_2 - (011)_2$ ii) $(73)_8 - (63)_8$	CO 2	3
(c)	Implement the following function by using Basic gates: $f = \bar{A}BCD + B\bar{C}\bar{D} + A\bar{C} + AB\bar{C}$	CO 2	3
(d)	Differentiate 1's and 2's complement methods of subtraction. Subtract following by using 1's and 2's complement methods of subtraction; i) $(1101)_2 - (1001)_2$ ii) $(33)_{10} - (27)_{10}$	CO 2	2,3
(e)	Convert the decimal numbers into binary and divide them in binary 55 ÷ 5	CO 2	3

Q. No 3	Attempt Any Four Parts. Each Question Carries 5 Marks.	CO	BL
(a)	Give classification of logic families. What parameters govern performance of logic family? Briefly explain each parameter.	CO 3	2
(b)	Explain tri-state output configuration of TTL logic family.	CO 3	2
(c)	Design AND gate, OR gate, NOR gate using NMOS.	CO 3	2,3
(d)	Explain working of ECL logic family.	CO 3	2
(e)	Explain the Tri-state Digital Buffer Data Bus Control with diagram.	CO 3	2

Q. No 4	Attempt Any Two Parts. Each Question Carries 10 Marks.	CO	BL
(a)	Simplify following by using K-Map and design the expression by using basic gates. i) $F = \sum_m (1, 3, 5, 7, 11, 12, 14, 15)$ ii) $F = \sum_m (0, 1, 4, 7, 9, 13, 15) + \sum_d (2, 8, 12)$	CO 4	3
(b)	Define and differentiate SOP and POS with the help of suitable example. Obtain minterms and maxterms for the following expressions: i) $f = \bar{A}BC + B\bar{C} + A\bar{C}$ ii) $f = (\bar{A} + B + C)(A + C)$	CO 4	2,3
(c)	Obtain truth-table for the following boolean expressions: *i)* $f = A\bar{C} + \bar{A}B + ABC$ *ii)* $f = (\bar{A} + \bar{B})(A + \bar{B} + \bar{C})$	CO 4	3

Q. No 5	Attempt Any Two Parts. Each Question Carries 10 Marks.	CO	BL
(a)	Draw the NAND gates-based full adder circuit with its truth table.	CO 5	
(b)	Draw the logic circuit of full subtractor with its truth table.	CO 5	
(c)	Explain working of 3:8 decoder with neat and clean diagram. Design following by using appropriate decoder: $F_1 = \sum m (1, 2, 3, , 7)$ $F_2 = \sum m (1, 5, 6)$ $F_3 = \sum m (1, 3, 5, 6)$	CO 5	2,4

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