Roll No. | | | | | | | | | | |

COER University

END SEMESTER EXAMINATION, EVEN SEM 2022-23

Time : 3 hours
Total Marks : 100
Program Name : B.Tech.(Hons.)-CSE, CSE(AI&ML), CSE(Cyber Security)
Semester : IV
Course Name : Computer Organization
Course Code : SOC202

Note: All questions are compulsory. No student is allowed to leave the examination hall before the completion of the time.

Q. No 1	Attempt Any Four Parts. Each Question Carries 5 Marks.	CO	BL
(a)	What are different types of register transfer operations?	CO 1	2
(b)	Explain Polling method of serial arbitration with its advantages and disadvantages.	CO 1	2
(c)	Compare Daisy chaining method and independent method of serial arbitration.	CO 1	2
(d)	Solve 5 *and* 4 using Booth's algorithm with flow chart.	CO 1	3
(e)	Explain the different types of cache memory mapping.	CO 1	2

Q. No 2	Attempt Any Four Parts. Each Question Carries 5 Marks.	CO	BL
(a)	Define hardwire and micro programmed control unit.	CO 2	1
(b)	Explain stack organization.	CO 2	2
(c)	What is cache memory?	CO 2	2
(d)	Define a detailed description of common bus system for four registers.	CO 2	1
(e)	Define read and write operations and describe memory transfer with diagram.	CO 2	1

Q. No 3	Attempt Any Four Parts. Each Question Carries 5 Marks.	CO	BL
(a)	What is Circular shift in Computer Architecture? Explain with the help of examples.	CO 3	2
(b)	Define addressing modes and explain: (i) Implied mode(ii) Immediate mode (iii) auto increment mode.	CO 3	2
(c)	Convert the following numbers as indicated. (a) $(110101)_2$ to unsigned base 10. (b) $(-29)_{10}$ to two's complement (use 8 bits in the result). (c) $(61543)_8$ to unsigned base 16 (use four base 16 digits in the result). (d) $(37)_{10}$ to unsigned base 3 (use four base 3 digits in the result).	CO 3	3
(d)	Explain parallel data transmission and serial data transmission.	CO 3	2
(e)	Explain multiple shared bus in computer architecture.	CO 3	2

Q. No 4	Attempt Any Two Parts. Each Question Carries 10 Marks.	CO	BL
(a)	Explain memory Hierarchy with characteristics.	CO 4	2
(b)	Define concept of paging in memory management hardware.	CO 4	1
(c)	We want to speed up computer performance with an additional unit for calculating in floating point format. This unit is 20 times faster than the same operations without unit. What percentage of a total computer time must this unit be active to achieve an overall increase in computer speed for 2.5 times?	CO 4	3

Q. No 5	Attempt Any Two Parts. Each Question Carries 10 Marks.	CO	BL
(a)	Analyze the basic concepts of pipelining with examples.	CO 5	4
(b)	Explain De-Morgan Theorem with the help of example.	CO 5	2
(c)	On a computer with a 32-bit memory address and the length of the memory location of 1 byte is installed set-associative cache. Cache size is 16 KB, block (line) size is 16 Bytes, set associative cache is 4-way. a) How many sets are there in cache? b) Which bits in the memory address determine the address of the set? c) Into which set is mapped the content of the memory address $10FFCFF_{(HEX)}$?	CO 5	3

End of Paper